
Contents

Biographies	xi
Acknowledgments	xiii
1 Introduction	1
1.1 Overview of WBG devices	2
1.1.1 WBG devices in comparison to Si devices	2
1.1.2 WBG device status	3
1.2 Motivation for WBG device characterization	9
1.3 About this book	11
References	13
2 Pulsed static characterization	17
2.1 Fundamentals of pulsed I – V testing	17
2.2 Test equipment description	18
2.3 Test fixture selection/design	20
2.4 Junction temperature control	21
2.5 Cryogenic device testing	25
2.6 Pulse waveform timing	29
2.7 Output (I_d – V_{ds}) characteristic	31
2.8 Transfer (I_d – V_{gs}) characteristic	35
2.9 Gate current ($I_{g,ss}$ – V_{gs}) characteristic	37
2.10 Drain-source leakage ($I_{d,off}$ – V_{ds}) characteristic	40
2.11 Summary	42
References	42
3 Junction capacitance characterization	43
3.1 Fundamentals of C – V testing	43
3.2 Test equipment description	45
3.3 Test fixture selection/design and calibration	47
3.4 Output capacitance (C_{oss}) characteristic	48
3.5 Input capacitance (C_{iss}) characteristic	51
3.6 Reverse transfer capacitance (C_{rss}) characteristic	53
3.7 Gate charge (Q_g) characteristic	54
3.8 Calculation of C_{oss} -related switching energies	59
3.9 Summary	62
References	63

4	Fundamentals of dynamic characterization	65
4.1	Switching commutation analysis	65
4.2	Fundamentals of DPT	69
4.3	DPT design	72
4.3.1	Load inductor	73
4.3.2	DC source	73
4.3.3	DC capacitor	74
4.3.4	Bleeder resistor	75
4.4	DPT control	75
4.5	Case study	77
4.5.1	Load inductor	77
4.5.2	DC source	78
4.5.3	DC capacitor bank	79
4.5.4	Bleeder resistor	80
4.5.5	DPT control	81
4.6	Summary	84
	References	84
5	Gate drive for dynamic characterization	87
5.1	Gate drive fundamentals	87
5.2	Gate drive-related key device characteristics	89
5.2.1	Gate drive design considering device static characteristics	90
5.2.2	Gate drive design considering device dynamic characteristics	92
5.3	Gate drive design	92
5.3.1	Signal isolator	93
5.3.2	Isolated power supply	97
5.3.3	Gate drive IC	99
5.3.4	Gate resistor	102
5.3.5	Decoupling capacitor	103
5.4	Case study	104
5.4.1	Signal isolator	104
5.4.2	Isolated power supply	106
5.4.3	Gate drive IC	107
5.4.4	Gate resistor	108
5.4.5	Decoupling capacitor	108
5.5	Summary	109
	References	109
6	Layout design and parasitic management	111
6.1	Impact of parasitics on the switching performance	111
6.1.1	Gate loop parasitics	111
6.1.2	Power loop parasitics	112
6.1.3	Common parasitics	114

6.2	DPT layout design	115
6.3	Case study	118
6.3.1	Brief overview of WBG devices' package	119
6.3.2	Case study 1: TO-247 package SiC MOSFETs	121
6.3.3	Case study 2: surface-mount WBG device	130
6.3.4	With consideration of current measurement in DPT	134
6.3.5	Gate drive	136
6.4	Summary	137
	References	138
7	Protection design for double pulse test	141
7.1	Overview of state-of-the-art protection scheme for WBG devices	141
7.2	Solid-state circuit breaker	144
7.2.1	Operation principle	145
7.2.2	Circuit implementation and design consideration	147
7.2.3	Test setup and procedure	151
7.2.4	Case study	152
7.3	Consideration for high-voltage WBG device DPT	158
7.3.1	Safety consideration	158
7.3.2	Protection scheme	158
7.4	Summary	160
	References	161
8	Measurement and data processing for dynamic characterization	165
8.1	Key considerations and challenges in dynamic characterization measurement	165
8.2	Oscilloscope selection and setup	166
8.3	Voltage probe selection and setup	167
8.4	Current sensor selection and setup	169
8.5	Time-alignment (deskew) of measurements	171
8.6	Consideration of CM ringing	173
8.7	Goals of dynamic data processing	174
8.8	Identification of switching transient subintervals	177
8.9	Calculation of I - V misalignment for deskew adjustment	183
8.10	Calculation of switching energy loss	187
8.11	Consideration of ringing and DC bias	191
8.12	Alternative method for switching energy loss calculation	194
8.13	Calculation of overshoot voltages and slew rates	196
8.14	Internal waveform estimation using static and dynamic results	198
8.15	Summary	204
	References	204
9	Cross-talk consideration	207
9.1	Mechanism causing cross-talk	208
9.2	Solutions for cross-talk suppression	211

9.2.1	Passive solutions	212
9.2.2	Active solutions	214
9.2.3	Summary of cross-talk suppression solutions	222
9.3	Methodology for characterization of cross-talk-related switching performance	222
9.3.1	Case study 1: GaN HEMT with passive solution	225
9.3.2	Case study 2: SiC MOSFET with active gate drive circuit	232
9.4	Summary	237
	References	238
10	Impact of three-phase system	241
10.1	Impacting factors and limitations in the actual three-phase system	242
10.1.1	Parasitics of inductive load	242
10.1.2	Interaction of phase-legs	247
10.1.3	Coupling effect by heat sink	250
10.1.4	Experimental verification	250
10.2	Dynamic characterization with practical application considerations	260
10.2.1	High-frequency modeling of inductive load	262
10.2.2	Basic idea for mitigation of adverse effect from inductive load	265
10.2.3	Design criteria of the auxiliary filter	265
10.2.4	Experimental verification	270
10.3	Case study: validation of the DPT results vs. switching performance in an actual system	274
10.3.1	Switching performance comparison between DPT board and three-phase VSC	276
10.3.2	Interaction of phase-legs and impact of heat sink on the switching performance	278
10.3.3	Validation of the accuracy of DPT results in comparison with switching performance in an actual converter	283
10.4	Summary	286
	References	287
11	Topology consideration	289
11.1	Current source converter	289
11.1.1	Switching commutation analysis	290
11.1.2	Comparison of switching commutation loop with conventional DPT	293

11.1.3	Consideration of other non-active devices	295
11.2	Three-level ANPC converter	295
11.2.1	Switching commutation analysis	297
11.2.2	Comparison of switching loop with conventional DPT	299
11.2.3	Consideration of other non-active devices	299
11.3	Discussion and summary	300
	References	301
Appendix A	Recommended equipment and components list for DPT setup	303
Appendix B	Data processing code for dynamic characterization	307
Index		327