

---

# Contents

---

|                                                                             |             |
|-----------------------------------------------------------------------------|-------------|
| <i>Preface</i>                                                              | <b>xi</b>   |
| <i>Acknowledgments</i>                                                      | <b>xiii</b> |
| <b>1 Introduction</b>                                                       | <b>1</b>    |
| 1.1 The general framework                                                   | 1           |
| 1.1.1 Why analog? Why digital?                                              | 1           |
| 1.1.2 Why low voltage?                                                      | 1           |
| 1.1.3 Why low power?                                                        | 2           |
| 1.1.4 Why CMOS?                                                             | 2           |
| 1.2 Techniques to reduce the power consumption and the voltage supply       | 2           |
| 1.2.1 Analog techniques                                                     | 2           |
| 1.2.2 Digital techniques                                                    | 4           |
| 1.3 Why floating gate MOS?                                                  | 6           |
| 1.4 FGMOS history                                                           | 7           |
| 1.5 Structure of the book                                                   | 11          |
| <b>2 The Floating Gate MOS transistor (FGMOS)</b>                           | <b>15</b>   |
| 2.1 Introduction                                                            | 15          |
| 2.2 The Floating Gate MOS (FGMOS) device                                    | 15          |
| 2.2.1 Introducing the device                                                | 15          |
| 2.2.2 Theory                                                                | 18          |
| 2.3 Designing with FGMOS: problems and solutions                            | 22          |
| 2.3.1 Simulation                                                            | 22          |
| 2.3.2 Charge accumulation                                                   | 28          |
| 2.4 Minimum input capacitance: implications to the total area of the device | 35          |
| 2.5 Summary and conclusions                                                 | 40          |
| Notation                                                                    | 40          |

|          |                                                                                                                |            |
|----------|----------------------------------------------------------------------------------------------------------------|------------|
| <b>3</b> | <b>FGMOS – Circuit applications and design techniques</b>                                                      | <b>43</b>  |
| 3.1      | Introduction                                                                                                   | 43         |
| 3.2      | Initial design ideas: three circuit equivalents for the FGMOS                                                  | 43         |
| 3.2.1    | FGMOS: a MOS transistor plus an adder                                                                          | 43         |
| 3.2.2    | FGMOS: a MOS transistor with a controllable threshold voltage                                                  | 44         |
| 3.2.3    | FGMOS in weak inversion: a current multiplier                                                                  | 45         |
| 3.3      | Circuits applications and design techniques                                                                    | 46         |
| 3.3.1    | A cascode current mirror                                                                                       | 46         |
| 3.3.2    | Two-stage OPAMP                                                                                                | 50         |
| 3.3.3    | FGMOS programmable inverter                                                                                    | 58         |
| 3.3.4    | An offset compensated FGMOS comparator                                                                         | 60         |
| 3.3.5    | FGMOS D/A converters                                                                                           | 66         |
| 3.3.6    | A programmable switched-current floating gate MOS cell                                                         | 73         |
| 3.4      | Summary and conclusions                                                                                        | 79         |
|          | Notation                                                                                                       | 81         |
| <b>4</b> | <b>Low power analog continuous-time filtering based on the FGMOS in the strong inversion ohmic region</b>      | <b>87</b>  |
| 4.1      | Introduction                                                                                                   | 87         |
| 4.2      | Transconductor basic blocks                                                                                    | 89         |
| 4.3      | The $G_m$ -C multiple-input linear integrator. Large signal description                                        | 91         |
| 4.3.1    | Operating point – design considerations                                                                        | 92         |
| 4.4      | The Common Mode Feedback Block (CMFB)                                                                          | 95         |
| 4.5      | Small signal considerations                                                                                    | 96         |
| 4.5.1    | The transconductance cell (N1)                                                                                 | 97         |
| 4.5.2    | The tuning amplifier (N2)                                                                                      | 99         |
| 4.5.3    | Common mode DC response                                                                                        | 101        |
| 4.6      | Second order effects                                                                                           | 103        |
| 4.6.1    | Total harmonic distortion                                                                                      | 103        |
| 4.7      | Power Supply Rejection Ratio (PSRR)                                                                            | 111        |
| 4.8      | Filter example                                                                                                 | 115        |
| 4.9      | Summary and conclusions                                                                                        | 117        |
|          | Notation                                                                                                       | 123        |
| <b>5</b> | <b>Low power analog continuous-time filtering based on the FGMOS in the strong inversion saturation region</b> | <b>129</b> |
| 5.1      | Introduction                                                                                                   | 129        |
| 5.2      | A $G_m$ -C integrator based on the FGMOS in the strong inversion saturation region for audio applications      | 130        |
| 5.2.1    | Design trade-offs. Power consumption, voltage supply and limits for the transconductance                       | 132        |

|          |                                                                                                                   |            |
|----------|-------------------------------------------------------------------------------------------------------------------|------------|
| 5.2.2    | The Common-Mode Feedback Circuit (CMFB): effects on the OTA performance                                           | 135        |
| 5.2.3    | Second-order effects                                                                                              | 143        |
| 5.2.4    | Power supply rejection ratio                                                                                      | 148        |
| 5.2.5    | A filter example                                                                                                  | 152        |
| 5.3      | An intermediate frequency FGMOS-based filter                                                                      | 157        |
| 5.3.1    | The FGMOS-based IF transconductor                                                                                 | 158        |
| 5.3.2    | The FGMOS cascode load and the CMFB                                                                               | 159        |
| 5.3.3    | Dynamic range                                                                                                     | 162        |
| 5.3.4    | Rejection to supply noise                                                                                         | 163        |
| 5.3.5    | A second-order filter prototype                                                                                   | 165        |
| 5.4      | A second-order FGMOS filter in a single poly technology                                                           | 168        |
| 5.4.1    | Effects of the metal-poly capacitors                                                                              | 168        |
| 5.4.2    | Experimental results                                                                                              | 173        |
| 5.5      | Comparison                                                                                                        | 175        |
|          | Notation                                                                                                          | 177        |
| <b>6</b> | <b>Low power analog continuous-time <math>G_m</math>-C filtering using the FGMOS in the weak inversion region</b> | <b>185</b> |
| 6.1      | FGMOS translinear principle                                                                                       | 186        |
| 6.2      | A $G_m$ -C FGMOS integrator using translinear circuits                                                            | 188        |
| 6.2.1    | The state-space integrator equations                                                                              | 188        |
| 6.2.2    | FGMOS blocks                                                                                                      | 189        |
| 6.2.3    | Second-order effects                                                                                              | 193        |
| 6.2.4    | A second-order filter example                                                                                     | 202        |
| 6.3      | Summary and conclusions                                                                                           | 207        |
|          | Notation                                                                                                          | 211        |
| <b>7</b> | <b>Low power log-domain filtering based on the FGMOS transistor</b>                                               | <b>215</b> |
| 7.1      | Log-domain integration with FGMOS                                                                                 | 216        |
| 7.1.1    | Basic principle                                                                                                   | 216        |
| 7.1.2    | Basic FGMOS circuits                                                                                              | 217        |
| 7.1.3    | The integrator                                                                                                    | 219        |
| 7.1.4    | Advantages and disadvantages of using FGMOS transistors                                                           | 221        |
| 7.2      | The second-order filter                                                                                           | 222        |
| 7.2.1    | The expander                                                                                                      | 224        |
| 7.2.2    | The input stage                                                                                                   | 225        |
| 7.3      | The common mode control                                                                                           | 225        |
| 7.4      | Design considerations. Second-order effects                                                                       | 226        |
| 7.4.1    | Multiple operating points in the filter                                                                           | 226        |
| 7.4.2    | Effect of the parasitic capacitances: qualitative study                                                           | 228        |
| 7.4.3    | Effect of $C_{GD}$ and the mismatch between the inputs: a quantitative study                                      | 229        |

|          |                                                                   |            |
|----------|-------------------------------------------------------------------|------------|
| 7.5      | A design example                                                  | 235        |
| 7.6      | Summary and conclusions                                           | 237        |
|          | Notation                                                          | 241        |
| <b>8</b> | <b>Low power digital design based on the FGMOS threshold gate</b> | <b>245</b> |
| 8.1      | Introduction                                                      | 245        |
| 8.2      | Threshold gates                                                   | 246        |
| 8.3      | The $\nu$ MOS threshold gate                                      | 247        |
| 8.3.1    | Theory                                                            | 247        |
| 8.3.2    | Practical design aspects                                          | 249        |
| 8.4      | $\nu$ MOS Threshold gates applications                            | 250        |
| 8.4.1    | Threshold logic based adders using floating-gate circuits         | 250        |
| 8.4.2    | $\nu$ MOS-based compressor designs                                | 255        |
| 8.4.3    | Sorting networks implemented as $\nu$ MOS circuits                | 258        |
| 8.4.4    | A multi-input Muller C-element                                    | 267        |
| 8.5      | Summary and conclusions                                           | 268        |
|          | Notation                                                          | 269        |
| <b>9</b> | <b>Summary and conclusions</b>                                    | <b>273</b> |
|          | <b>References</b>                                                 | <b>279</b> |
|          | <b>Index</b>                                                      | <b>297</b> |